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HOST CONTROL INTERFACE AND REGISTERS AIDED CONTINUOUSLY PROGRAMMABLE FIR FILTER DESIGN FOR NON-LINEAR DSP APPLICATIONS

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ABSTRACT

This paper aims to design a continuously programmable digital finite impulse response(CPDF FIR) filter for non-linear signal filtering resolutions. The proposed CPDF FIR filter encompasses input block, host-control interface (HCI), register blocks aided parallel filter module, and an output block. The inputincepts with non-linear sequentially repeating chirp signal, which is subsequently processed for frame based (floating to fixed) sample generation and delay insertion. Here one sample per frame is used to avoid sample overflow and quantization error with the introduction of one clock delay. Consequently, the delayed sampled signal was subsequently processed using register block which functions in unification with HCI. Here, HCI helps in coefficient updates as well as low-pass coefficient assignment to the Butterworth direct discrete FIR filter for reference signal generation. On the other hand, it helps continuous coefficient update to the register block. Prominently, the register block uses low pass coefficients to filter each chirp signal or delayed samples in the beginning, followed by high-pass filter coefficient using direct discrete FIR filter model. CPDF with linear and differential optimization approach are used for coefficient updates. The overall work exposes that the proposed CPDF FIR filter accomplishes optimal filtering performance with low area, minimum hardware consumption such as reduced multipliers(43) and adder/subtractors(42). Furthermore, it exhibits significantly low delay of 6.166 ns. Such robustness indicates suitability of the CPDF-FIR filter towards varied non-linear filtering applications including industrial IoT data filtering or speech signals.

KEYWORDS: *Continuously Programmable digital filter, fir filter, host control interface, delay insertion, parallel fir, multiplier reduction*